In the Claims

1. (Currently Amended) The memory agent according to claim 12 further ~~A memory agent~~ comprising:

~~a receive link interface having a plurality of receive lanes to receive training sequences;~~

~~a transmit link interface having a plurality of transmit lanes to transmit return sequences; and~~

a loopback unit coupled to the first receive and first transmit link interfaces to selectively redirect one or more of the plurality of first receive lanes to one or more of the plurality of first transmit lanes to retransmit the plurality of ~~received~~ training sequences as the plurality of return sequences during the ~~a lane~~ testing operation.

2. (Currently Amended) The memory agent according to claim 1 ~~wherein:~~

~~the receive link interface is a first receive link interface;~~

~~the transmit link interface is a first transmit link interface; and~~ further comprising:

a second transmit link interface having a plurality of second transmit lanes; and

a second receive link interface having a plurality of second receive lanes.

3. (Currently Amended) The memory agent according to claim 2 wherein

the memory agent operates ~~may operate~~ in a passthrough mode during the ~~a lane~~ testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface.

4. (Currently Amended) The memory agent according to claim 1 wherein the memory agent selectively maps ~~may selectively map~~ one of the plurality of first receive lanes to more than one of the plurality of first transmit lanes during the ~~a lane~~ testing operation.

5. (Currently Amended) The memory agent according to claim 1 wherein the memory agent selectively maps ~~may selectively map~~ one or more of the plurality of first receive lanes to one or more of the plurality of first transmit lanes according to ~~a~~ one of the plurality of mappings.

6. (Currently Amended) The memory agent according to claim 5 wherein the memory agent selects ~~may select~~ one of the plurality of mappings responsive to one of the mapping indicators ~~a mapping indicator in a training sequence received on the receive link interface~~.

7. (Currently Amended) The memory agent according to claim 1 wherein the memory agent retransmits one of ~~may retransmit~~ the plurality of ~~received~~ training sequences with modification as the corresponding one of the plurality of return sequences.

8. (Currently Amended) The memory agent according to claim 1 wherein the memory agent further comprises a memory buffer.

9. (Currently Amended) The memory agent according to claim 1 wherein the memory agent further comprises a memory module.

10. (Cancelled)

11. (Previously Presented) The memory agent according to claim 1 wherein the loopback unit comprises a multiplexer.

12. (Currently Amended) A memory agent comprising:

a first receive link interface having a plurality of first receive lanes; and

a ~~second~~ first transmit link interface having a plurality of ~~second~~ first transmit lanes;

wherein the memory agent: ~~agent may:~~

receives a plurality of ~~transmit~~ training sequences having different mapping indicators on ~~one or more of~~ the plurality of first receive lanes during a testing operation;

transmits a plurality of ~~receive~~ return sequences on ~~one or more of~~ the plurality of ~~second~~ first transmit lanes wherein each of the plurality of return sequences is responsive to a corresponding one of the plurality of ~~the~~ training sequences according to a corresponding one of a plurality of mappings during the testing operation; and

analyzes ~~analyze~~ the return sequences based on the plurality of mappings to identify failed lanes in the plurality of first receive lanes and the plurality of ~~second~~ first transmit lanes.

13. (Cancelled)

14. (Currently Amended) The memory agent according to claim 12 wherein:

the plurality of first receive lanes comprises receive bit lanes; and

the plurality of ~~second~~ first transmit lanes comprises transmit bit lanes.

15. (Cancelled)

16. (Currently Amended) The memory agent according to claim 12 wherein the memory agent transmits ~~may transmit~~ test parameters in the plurality of training sequences.

17. (Currently Amended) The memory agent according to claim 12 wherein the memory agent transmits ~~may transmit~~ electrical stress patterns in the plurality of training sequences.

18. (Currently Amended) The memory agent according to claim 12 wherein the memory agent is coupled to ~~comprises~~ a memory controller.

19. (Previously Presented) A method comprising:

transmitting a first training sequence to a memory agent on a first plurality of lanes during a testing operation;

transmitting a first return sequence from the memory agent on a second plurality of lanes responsive to the first training sequence according to a first mapping during the testing operation;

transmitting a second training sequence to the memory agent on the first plurality of lanes during the testing operation;

transmitting a second return sequence from the memory agent on the second plurality of lanes responsive to the second training sequence according to a second mapping during the testing operation; and

analyzing the return sequences based on the first and second mappings.

20. (Previously Presented) The method according to claim 19 further comprising:

redirecting the first training sequence to the second plurality of lanes as the first return sequence during the testing operation; and

redirecting the second training sequence to the second plurality of lanes as the second return sequence during the testing operation.

21. (Previously Presented) The method according to claim 20 further comprising:

passing the first training sequence through the memory agent to a third plurality of lanes during the testing operation;

passing the second training sequence through the memory agent to a third plurality of lanes during the testing operation;

passing the first return sequence from a fourth plurality of lanes through the memory agent to the second plurality of lanes during the testing operation; and

passing the second return sequence from the fourth plurality of lanes through the memory agent to the second plurality of lanes during the testing operation.

22. (Previously Presented) The method according to claim 19 wherein the first return sequence comprises one or more groups that are substantially the same as one or more groups in the first training sequence.

23. (Previously Presented) The method according to claim 19 wherein the second return sequence comprises one or more groups that are substantially the same as one or more groups in the second training sequence.

24. (Previously Presented) The method according to claim 19 wherein the first training sequence comprises a mapping indicator.

25. (Previously Presented) The method according to claim 19 wherein the first training sequence comprises an electrical stress pattern.

26. (Previously Presented) The method according to claim 19 wherein the memory agent comprises a memory module.

27. (Previously Presented) The method according to claim 19 wherein the memory agent comprises a memory buffer.

28. (Currently Amended) The memory agent according to claim 12 further ~~A memory system~~ comprising:

~~memory agent comprising:~~

~~a receive link interface having a plurality of receive lanes to receive training sequences;~~

~~a transmit link interface having a plurality of transmit lanes to transmit return sequences; and~~

a loopback unit coupled to the first receive and first transmit link interfaces to selectively redirect one or more of the plurality of first receive lanes to one or more of the plurality of first transmit lanes to retransmit the plurality of ~~received~~ training sequences as the plurality of return sequences during the ~~a lane~~ testing operation, wherein ~~; and~~

a memory controller is coupled to the memory agent.

29. (Cancelled)

30. (Currently Amended) The memory system according to claim 28 wherein:
the ~~first~~ plurality of first receive lanes comprises receive bit lanes; and
the ~~second~~ plurality of first transmit lanes comprises transmit bit lanes.

31. (Currently Amended) The memory system according to claim 28 wherein ~~further comprising~~ a second memory agent is coupled to the memory agent.

32. (Previously Presented) The memory agent according to claim 7 wherein the modification includes identifying or status information.

33. (Currently Amended) The memory agent according to claim 1 wherein one of the plurality of return sequences comprises one of the plurality of ~~received~~ training sequences.

34. (Currently Amended) The memory agent according to claim 1 wherein one of the plurality of return sequences consists essentially of one of the plurality of ~~received~~ training sequences.